

A unified architecture for quantum lookup tables

2406.18030

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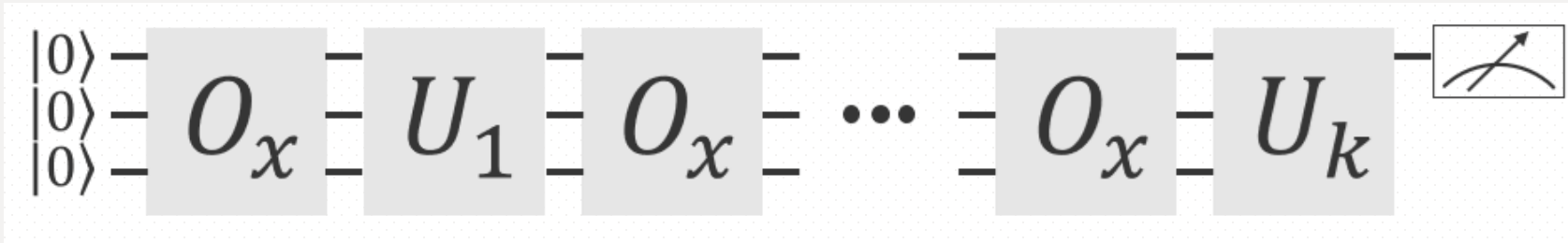
What is quantum lookup table

- It stores **classical data** and allows queries to be made in superposition
- It is a general-purpose architecture for the implementation of unstructured quantum oracles

$$|i\rangle|b\rangle \longrightarrow O_x \longrightarrow |i\rangle|b \cdot x_i\rangle$$

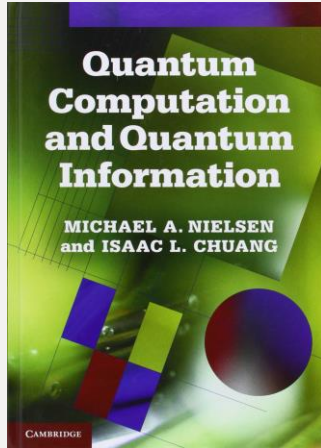
Why quantum lookup table?

- Most quantum algorithms are naturally phrased as oracle query algorithms



- Oracle provides description of Hamiltonian in quantum simulation
- Oracle encodes classical datasets into quantum state in quantum machine learning
- Essential to achieve quantum computational advantage
 - Quantum state preparation is expensive; the overhead may negate the quantum advantage

Prior arts



Fan-out

PHYSICAL REVIEW X **8**, 041015 (2018)

Encoding Electronic Spectra in Quantum Circuits with Linear T Complexity

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QROM

PHYSICAL REVIEW A **78**, 052310 (2008)

Architectures for a quantum random access memory

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(Received 7 August 2008; published 5 November 2008)

QRAM

 quantum
the open journal for quantum science

PAPERS

PERSPECTIVE

Trading T gates for dirty qubits in state preparation and unitary synthesis

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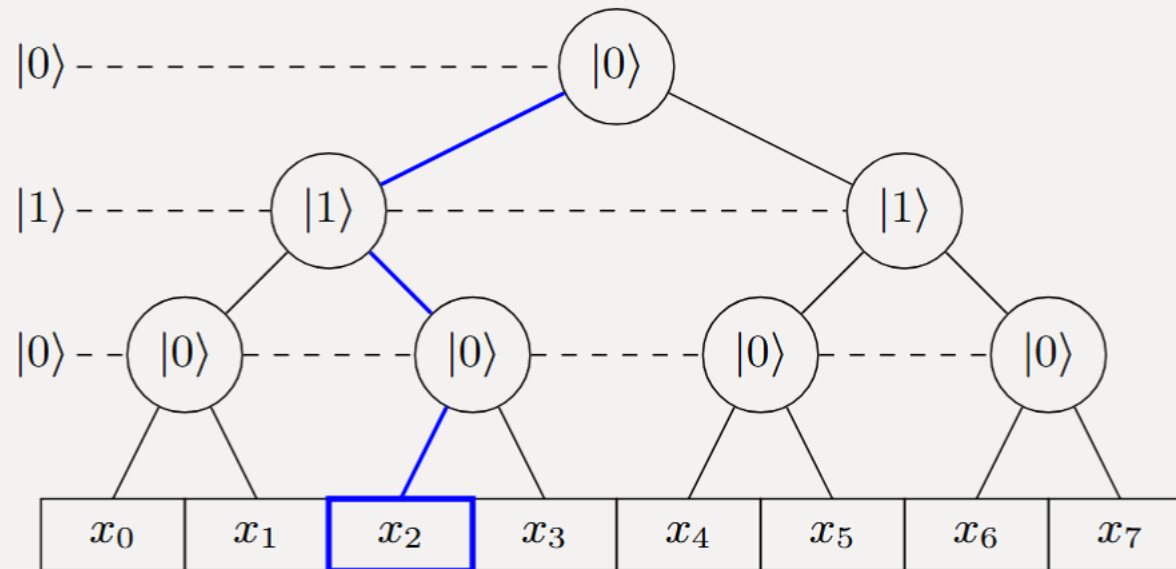
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SELECT-SWAP

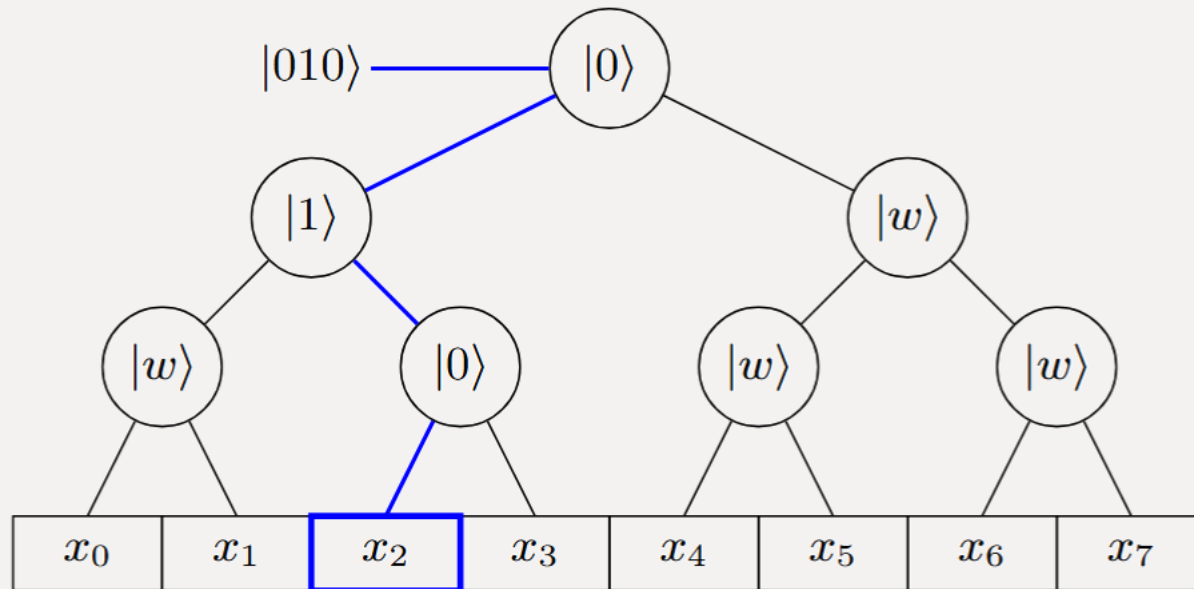
Duke

Fan-out architecture

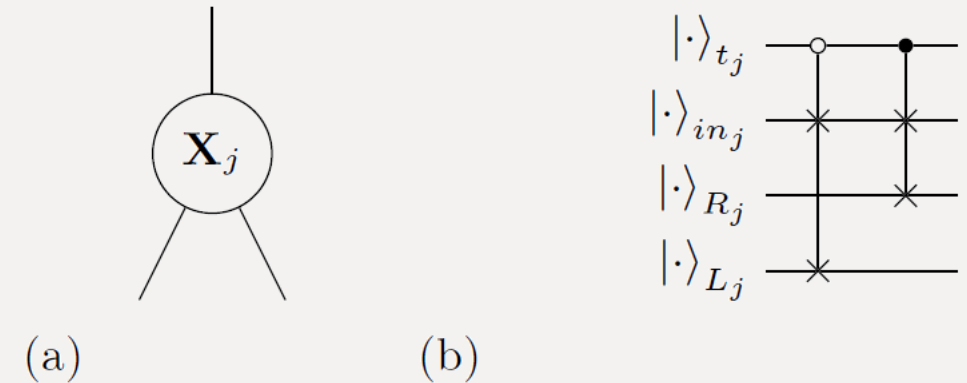


- Linear infidelity

Bucket-brigade (QRAM) architecture



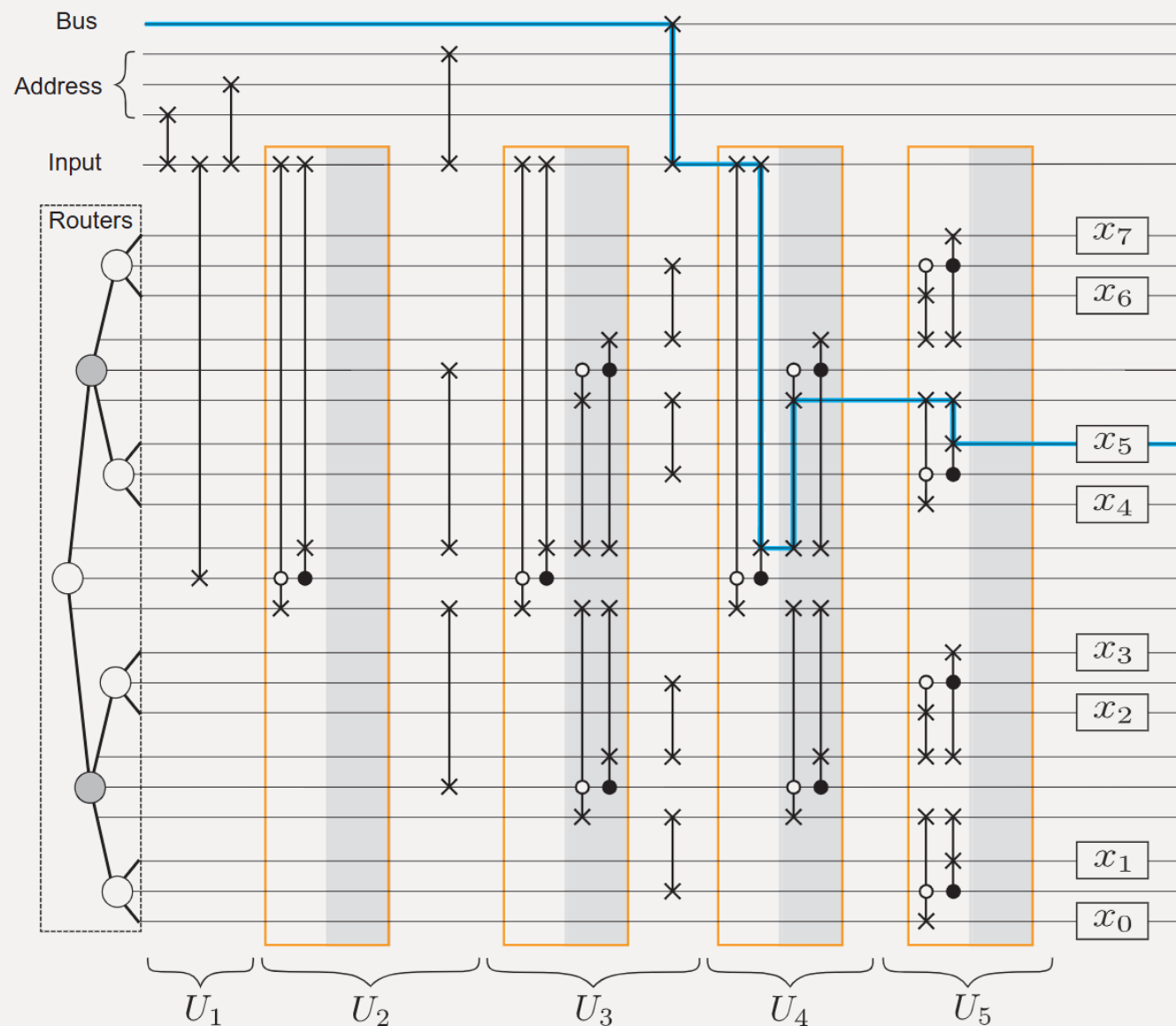
CSWAP router



- Low query time $O(\log N)$
- Low infidelity $O(\log^2 N)$
- High T-gate count: $O(N)$

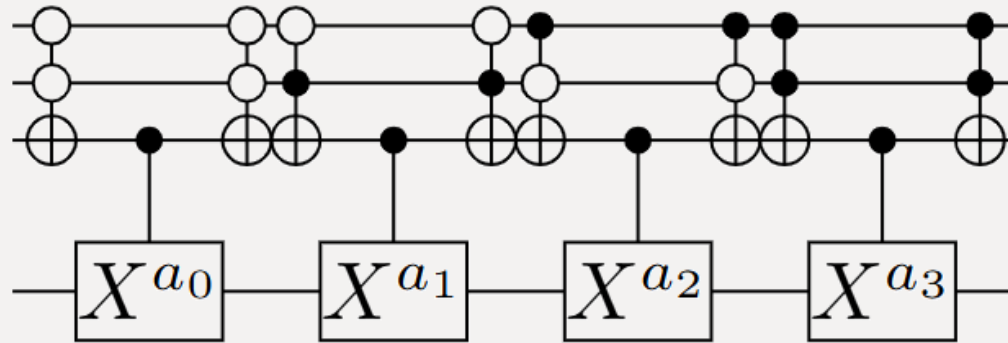
Giovannetti, Vittorio, Seth Lloyd, and Lorenzo Maccone. "Architectures for a quantum random access memory." *Physical Review A* 78, no. 5 (2008): 052310.
 Hann, Connor T., Gideon Lee, S. M. Girvin, and Liang Jiang. "Resilience of quantum random access memory to generic noise." *PRX Quantum* 2, no. 2 (2021): 020311.

Bucket-brigade (QRAM) circuit



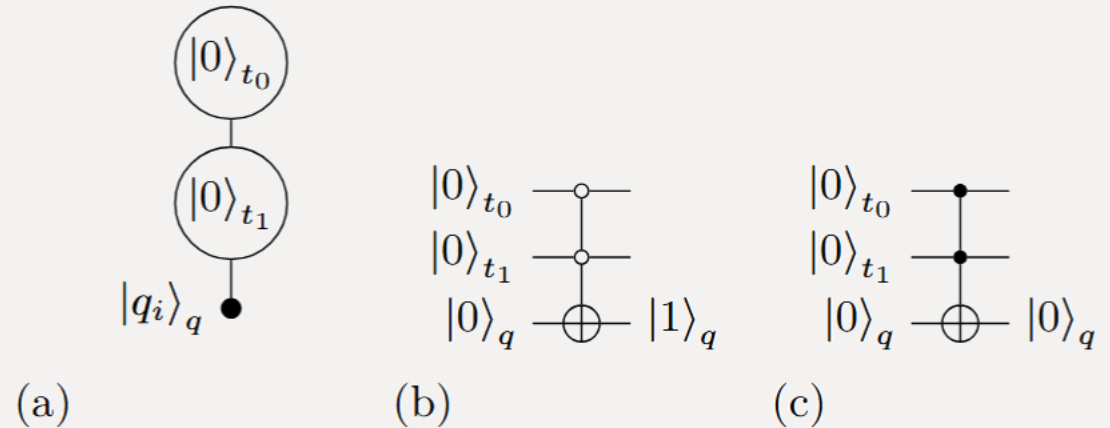
- All-to-all connectivity assumption
- Assume same gate error

QROM architecture

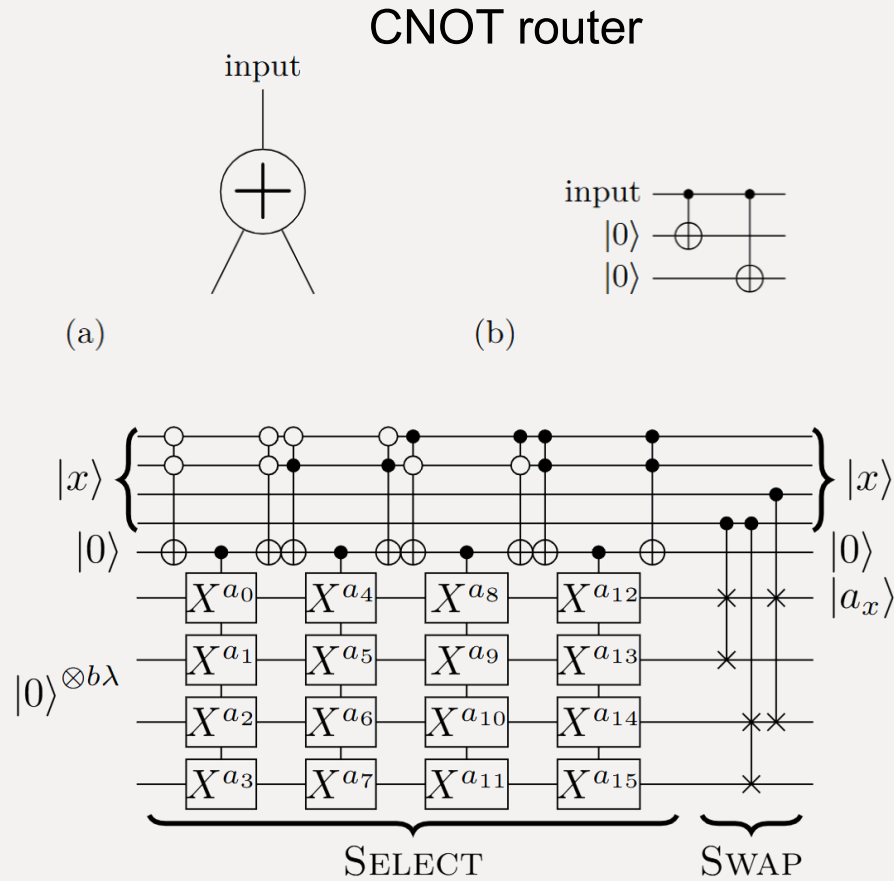
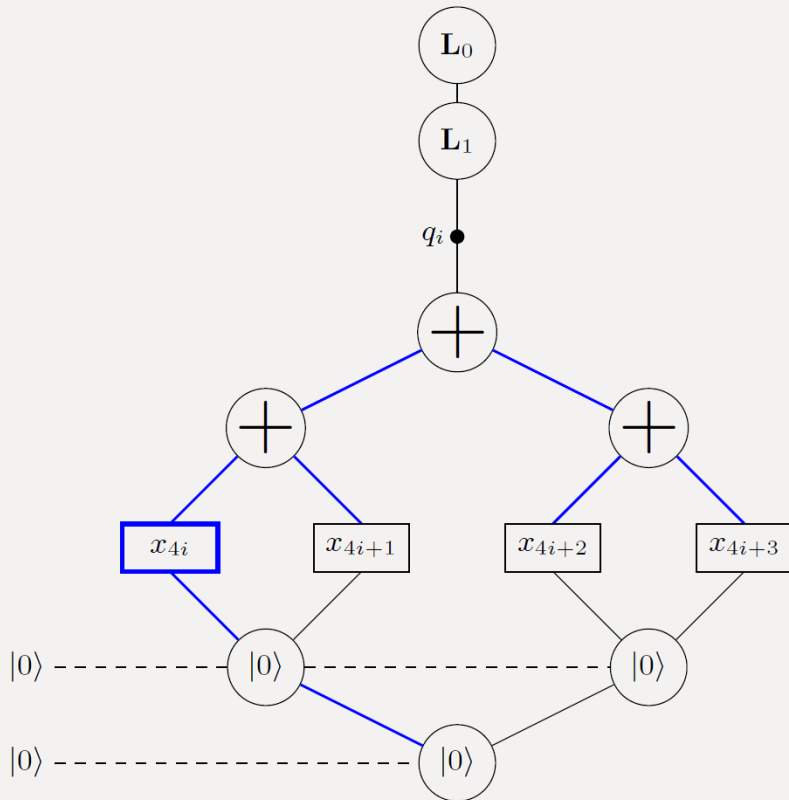


- Low qubit count $O(\log N)$
- High query time $O(N)$
- High infidelity $O(N)$
- High T-gate count: $O(N)$

Linear router



SELECT-SWAP architecture



- Sublinear qubit count $O(\sqrt{N})$
- Sublinear query time $O(\sqrt{N})$
- Fixed high infidelity $O(N)$
- Sublinear T-gate count: $O(\sqrt{N})$

Summary of prior art

Architecture	Infidelity	Query-depth	Qubits	T-gates	Layout
QRAM [19, 24]	$O(\log^2 N)$	$O(\log N)$	$O(N)$	$O(N)$	all-to-all
QROM [4]	$O(bN)$	$O(N)$	$O(\log N + b)$	$O(N)$	all-to-all ^a
SELECT-SWAP [23]	$O(bN)$	$O(\frac{N}{\lambda} + \log \lambda)$	$O(\log N + b\lambda)$	$O(\frac{N}{\lambda} + b\lambda)$	all-to-all

- Can we drop the all-to-all assumption in the analysis?
- Can we preserve the good properties from all these frameworks?

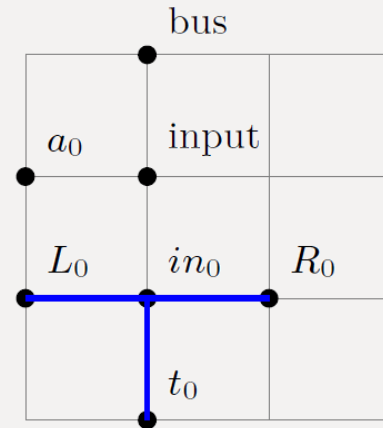
Our result

Architecture	Infidelity	Query-depth	Qubits	T-gates	Layout
QRAM [19, 24]	$O(\log^2 N)$	$O(\log N)$	$O(N)$	$O(N)$	all-to-all
QROM [4]	$O(bN)$	$O(N)$	$O(\log N + b)$	$O(N)$	all-to-all ^a
SELECT-SWAP [23]	$O(bN)$	$O(\frac{N}{\lambda} + \log \lambda)$	$O(\log N + b\lambda)$	$O(\frac{N}{\lambda} + b\lambda)$	all-to-all
general single-bit (Sec. III)	$\tilde{O}(\frac{\gamma N}{\lambda})$	$O(\frac{N}{\lambda} \log N)$	$O(\log \frac{N}{\lambda} + \lambda)$	$O(\frac{N}{\gamma} + \frac{N}{\lambda} \log \frac{N}{\lambda} + \lambda)$	local, planar
general multi-bit parallel (Sec. V)	$\tilde{O}(\frac{b\gamma N}{\lambda})$	$O(\frac{N}{\lambda} (\log bN))$	$O(\log \frac{N}{\lambda} + b\lambda)$	$O(\frac{N}{\lambda} \log \frac{N}{\lambda} + \frac{bN}{\gamma} + b\lambda)$	local, planar
general multi-bit sequential (Sec. V)	$\tilde{O}(\frac{b\gamma N}{\lambda} + b^2)$	$O(\frac{N}{\lambda} \log(bN) + b)$	$O(\log \frac{N}{\lambda} + b\lambda)$	$O(\frac{N}{\gamma} + \frac{N}{\lambda} \log \frac{N}{\lambda} + b\lambda)$	local, planar
single-bit (Sec. III)	$\tilde{O}(N^{3/4})$	$O(\sqrt{N} \log N)$	$O(\sqrt{N})$	$O(N^{3/4})$	local, planar
parallel multi-bit (Sec. V)	$\tilde{O}(bN^{3/4})$	$O(\sqrt{N} \log N)$	$O(b\sqrt{N})$	$O(bN^{3/4})$	local, planar
sequential multi-bit (Sec. V)	$\tilde{O}(bN^{3/4} + b^2)$	$O(\sqrt{N} \log(bN) + b)$	$O(b\sqrt{N})$	$O(N^{3/4} + b\sqrt{N})$	local, planar

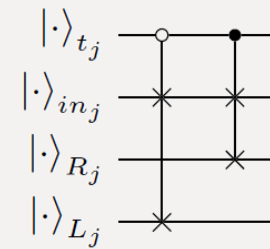
- Planar layout
- Sublinear scalings for local connectivity
- Fine-tuned error dependence
- Unified framework
- Extend to large word size

Error type	Error rate symbol
Idling	ε_I
Qubit	ε_Q
Long range	ε_L
SWAP gate	ε_s
CSWAP gate	ε_{cs}
CNOT gate	ε_c
CCNOT gate	ε_{cc}

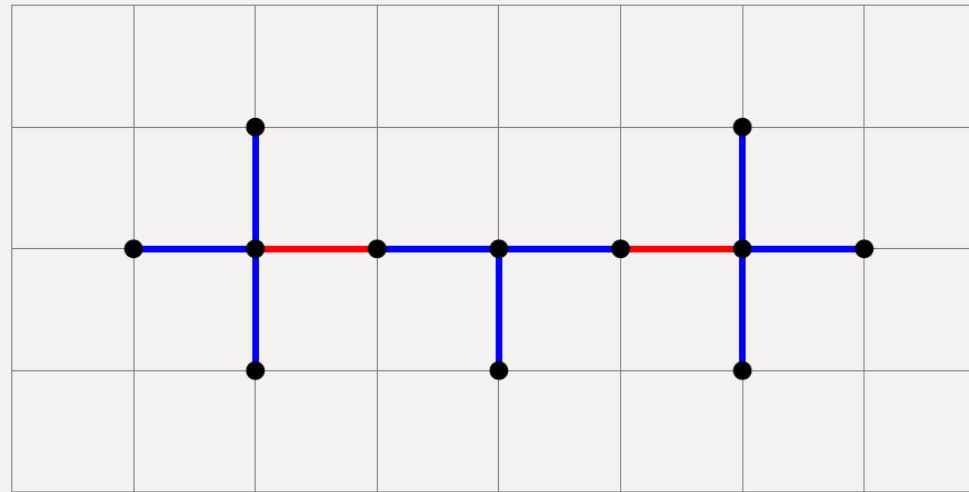
Planar layout for single CSWAP router



(a)

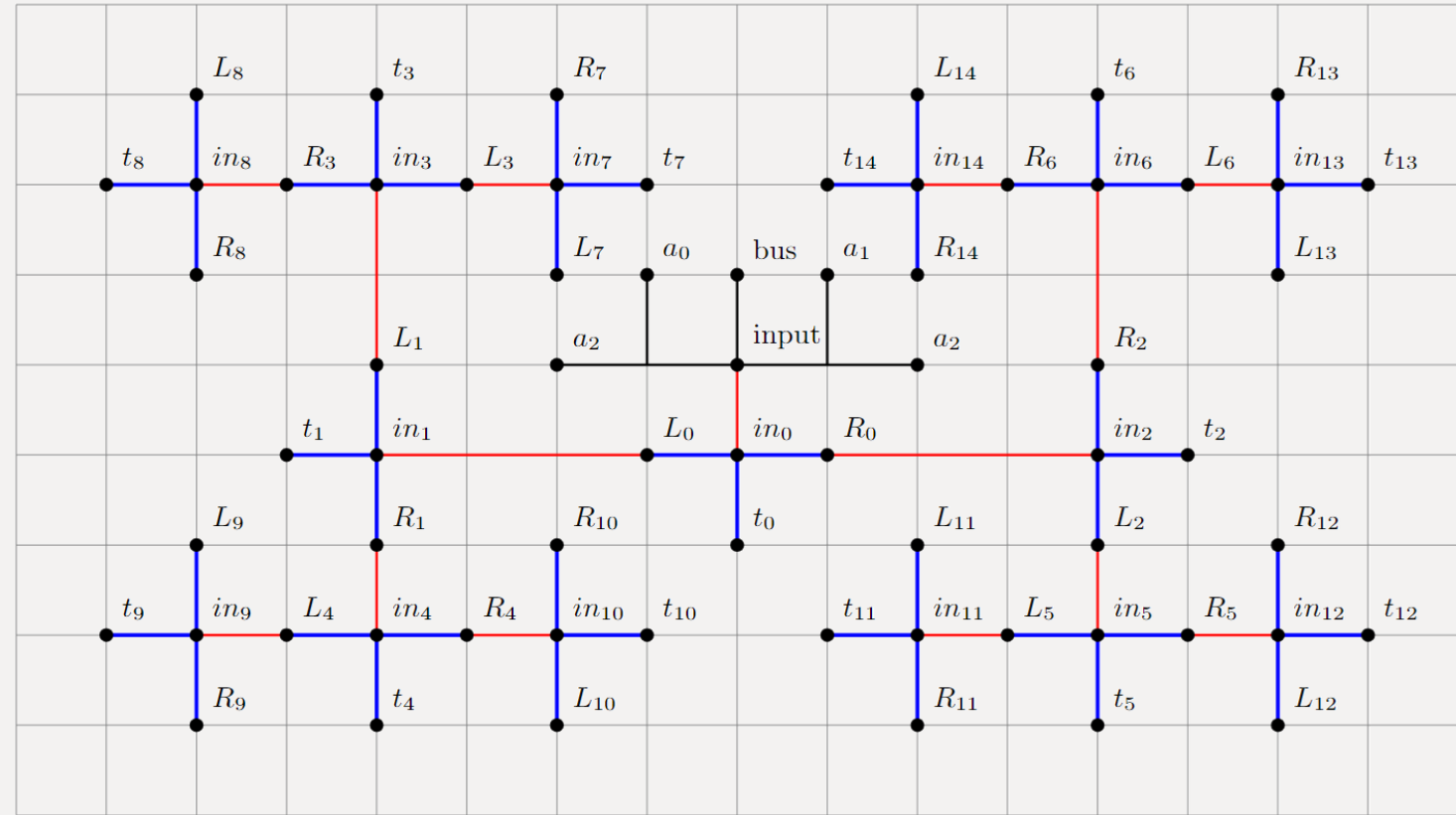
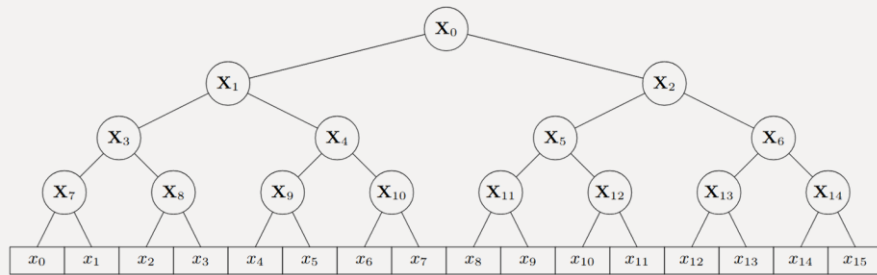


(b)



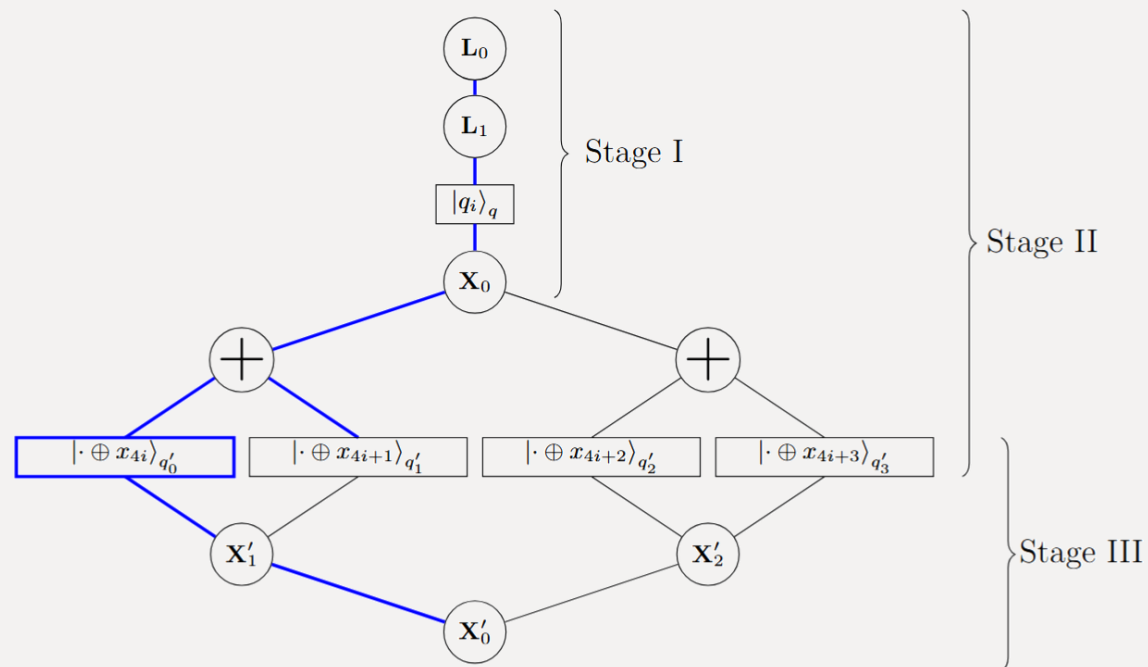
(c)

Planar layout for QRAM



- This layout can be extended to our unified framework.

Ideal construction



Algorithm 1 Pseudocode for quantum data lookup on memory of size N , partition size λ , and CNOT tree size γ . This corresponds to the high-level routing scheme shown in Figure 8. SETROUTER(a, r) sets the address bit(s) a to router(s) of type $r \in \{\mathbf{X}, \mathbf{L}\}$ as described in Section II. For each SETROUTER operation, a path connected by its corresponding routers is formed. ROUTEDATA(d, p) moves data qubit d from one end to the other end of the path p . We use $\bar{p}$ to denote the reverse of the path p .

Setup: classical database **data** of size N with $n = \log_2 N$, memory partition $\lambda \leq N$ with $d = \log_2 \left(\frac{N}{\lambda}\right)$ and CNOT tree size $\gamma \leq \lambda$ with $d' = \log_2 \left(\frac{\lambda}{\gamma}\right)$.

Input: state $|a\rangle_{\text{add}}$ where $a = a_0 \dots a_{n-1}$ is an address of length n .

Output: state $|a\rangle_{\text{add}} |\text{data}[a]\rangle_{\text{out}}$ where **data**[a] refers to the data at address a .

Stage I:

- 1: Initialize all registers of the quantum lookup table to $|0\rangle$.
- 2: SETROUTER($a_0 \dots a_{d-1}, \mathbf{L}$) ▷ Set d linear routers $\mathbf{L}_k$
- 3: SETROUTER($a_d \dots a_{d+d'-1}, \mathbf{X}$) ▷ Set d' CSWAP routers $\mathbf{X}$ in the corresponding path p_1 of the CSWAP tree

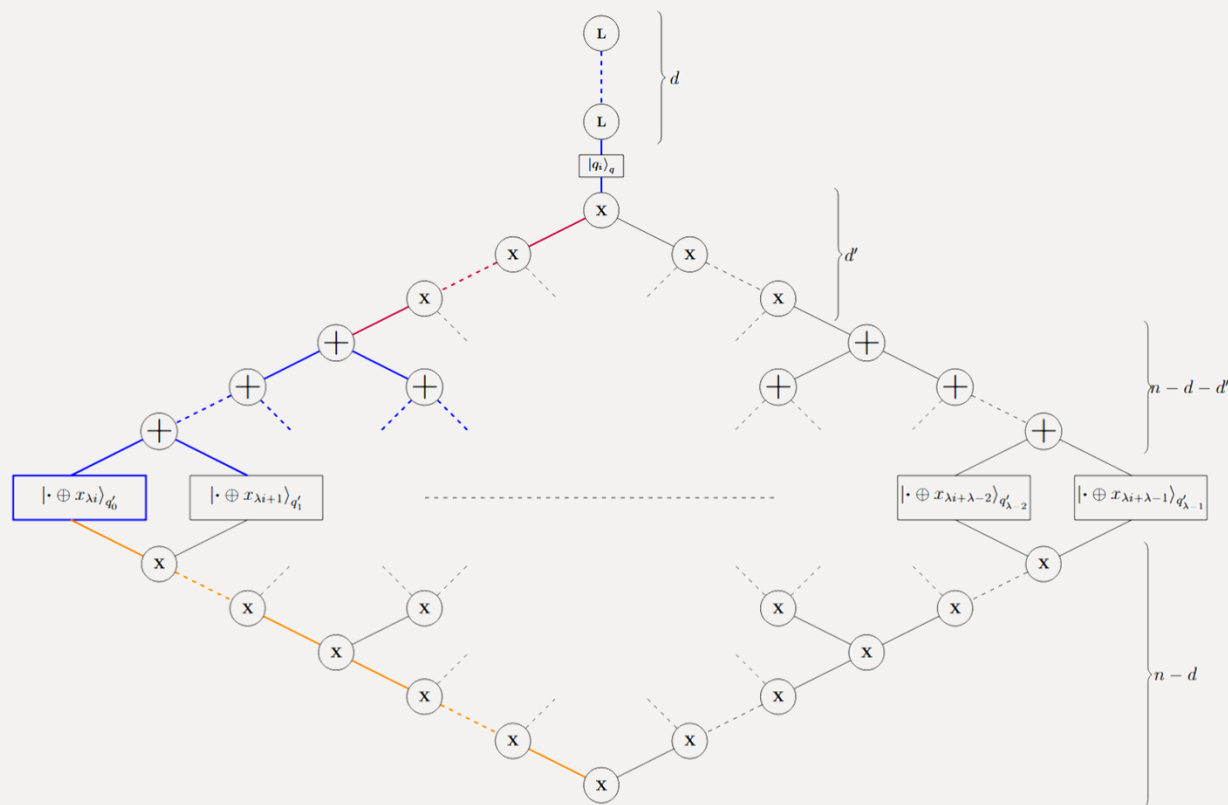
Stage II:

- 4: **for** i in $0 \dots 2^d - 1$ **do**
- 5: **if** $i = a_0 \dots a_{d-1}$ **then** ▷ The state of Linear routers $\mathbf{L}$ determines the activation qubit q_i at round i
- 6: Set $|q_i\rangle_q \leftarrow |1\rangle$
- 7: **else**
- 8: Set $|q_i\rangle_q \leftarrow |0\rangle$
- 9: ROUTEDATA(q_i, p_1) ▷ Route q_i along the path p_1 determined by the CSWAP routers to a CNOT router
- 10: Propagate q_i 's signal to the γ leaves $|c_0, \dots, c_{\gamma-1}\rangle_{q'}$ of the CNOT tree.
- 11: **for** j in $0 \dots \lambda - 1$ **do** ▷ Set the q' registers determined by q_i and **data**
- 12: Apply unitary $U_{\lambda \cdot i + j}$ where $U_{\lambda \cdot i + j} = \text{CNOT}[c_j] |q'_j\rangle$ if **data**[$\lambda \cdot i + j$] = 1 and **I** otherwise.
- 13: Reset all qubits c_j and those in the CNOT tree to 0.
- 14: ROUTEDATA($q_i, \bar{p}_1$) ▷ Route q_i back up the CSWAP routers to its original location
- 15: Reset all the qubits of the CSWAP routers except the router status qubits and q_i to 0.

Stage III:

- 16: SETROUTER($a_d \dots a_{n-1}, \mathbf{X}$) ▷ Set the status of $\log_2(\lambda)$ CSWAP in path p_2 routers based on the remaining address bits
- 17: ROUTEDATA(q'_ℓ, p_2), $\ell = a_d \dots a_{n-1}$ ▷ Route q'_ℓ along the query path p_2 set by the CSWAP routers to the output register

Main result



Theorem III.1. *Consider the quantum data lookup structure with the high-level scheme in Fig. 8 with N memory locations. Let $n = \log N$, $\lambda = 2^{n-d}$ be the partition size and $\gamma = 2^{n-d-d'}$ be the size of a CNOT tree with $d' \leq d \leq n$. The infidelity of this circuit is*

$$\begin{aligned}
& O\left(\varepsilon_L \left(\frac{\gamma N}{\lambda} + \frac{N}{\lambda} \log \frac{\lambda}{\gamma}\right) + \varepsilon_s \log \frac{\lambda^2}{\gamma}\right. \\
& + \varepsilon_I \left(\frac{N}{\lambda} \log N \left(\log \frac{N}{\gamma} + \gamma + \log \frac{\lambda}{\gamma}\right) + \text{polylog } \lambda\right) \\
& + \varepsilon_c \frac{\gamma N}{\lambda} + \varepsilon_{cc} \frac{N}{\lambda} \log \frac{N}{\lambda} \\
& \left. + \varepsilon_{cs} \left(\frac{N}{\lambda} \log \frac{\lambda}{\gamma} + \log^2 \frac{\lambda}{\gamma} + \log^2 \lambda\right)\right). \tag{3}
\end{aligned}$$

Moreover, the T count for this design is $O(\frac{N}{\gamma} + \frac{N}{\lambda} \log \frac{N}{\lambda} + \lambda)$, and its qubit count is $O(\log \frac{N}{\lambda} + \lambda)$.

Moreover, the T count for this design is $O(\frac{1}{N})$.

Duke

Current progress in the field

Demonstrating Coherent Quantum Routers for Bucket-Brigade Quantum Random Access Memory on a Superconducting Processor

Sheng Zhang,^{1,2,3} Yun-Jie Wang,⁴ Peng Wang,^{1,2,3} Ren-Ze Zhao,^{1,2} Xiao-Yan Yang,^{1,2} Ze-An Zhao,^{1,2} Tian-Le Wang,^{1,2} Hai-Feng Zhang,^{1,2} Zhi-Fei Li,^{1,2} Yuan Wu,^{1,2} Hao-Ran Tao,⁵ Liang-Liang Guo,⁵ Lei Du,⁵ Chi Zhang,⁵ Zhi-Long Jia,⁵ Wei-Cheng Kong,⁵ Zhuo-Zhi Zhang,^{1,2,3} Xiang-Xiang Song,^{1,2,3} Yu-Chun Wu,^{1,2,6} Zhao-Yun Chen,^{6,*} Peng Duan,^{1,2,†} and Guo-Ping Guo^{1,2,5,‡}

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(Dated: June 1, 2025)

A distillation–teleportation protocol for fault-tolerant QRAM

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Productionizing Quantum Mass Production

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³ Department of Computer Science, University of Toronto, Toronto, ON, Canada

⁴ Pacific Northwest National Laboratory, Richland, WA, USA

(Dated: June 6, 2025)

- How to benefit from qutrit/qudit.
- How to do QRAM simulation on a real machine to gain better intuition.
- If the distillation-teleportation's bottleneck is classical, can we improve it to make it work?
- Dream: $O(\log N)$ infidelity for planar layout.